

FIGURE 1

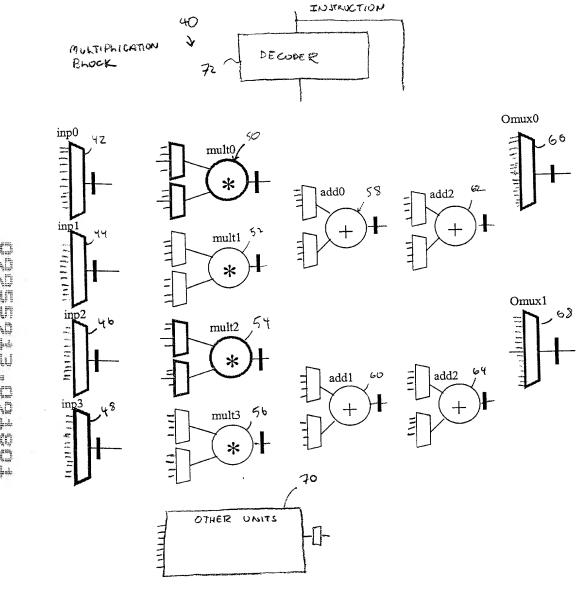


FIGURE 2

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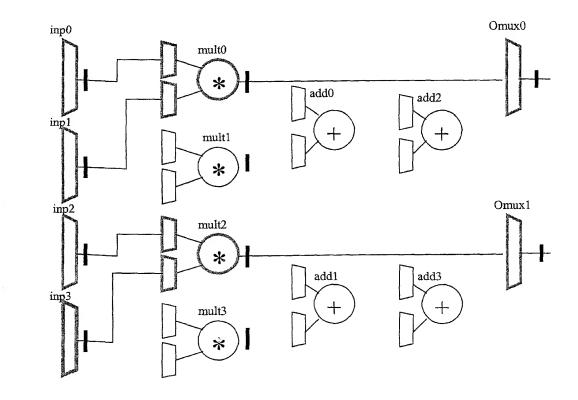
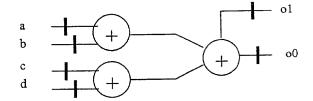


FIGURE 3A

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4ADD32 – Sum of 4 32-bit inputs



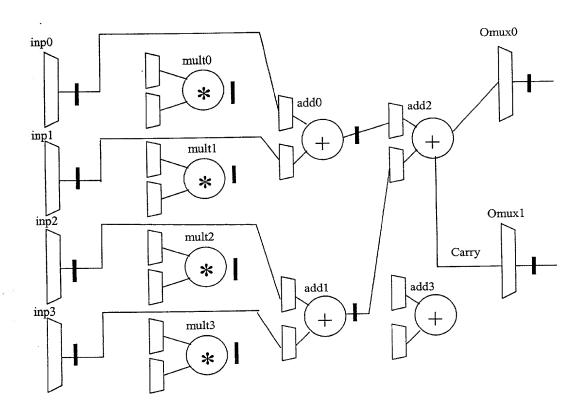


FIGURE 3B

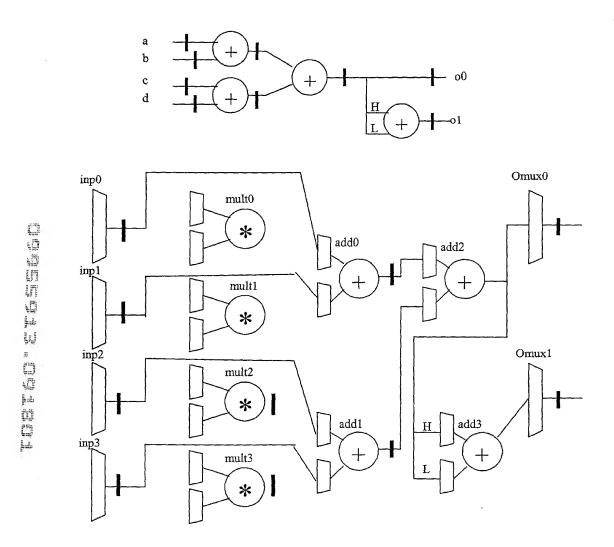
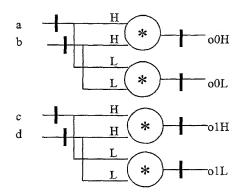


FIGURE 3C

4MULT – 4 multipliers with pack 16-bit inputs



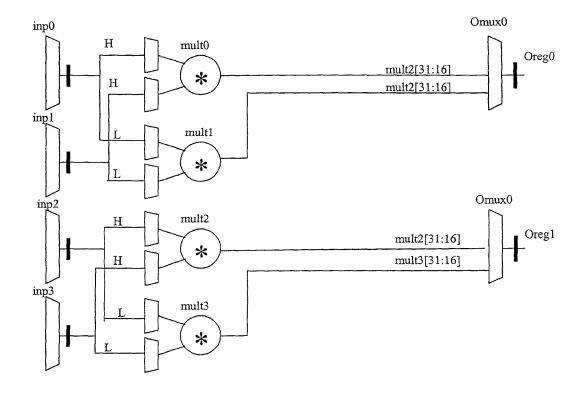
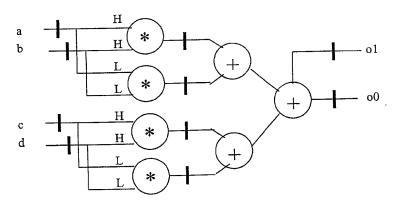


FIGURE 30

4MULTSUM – Sum of 4 multipliers



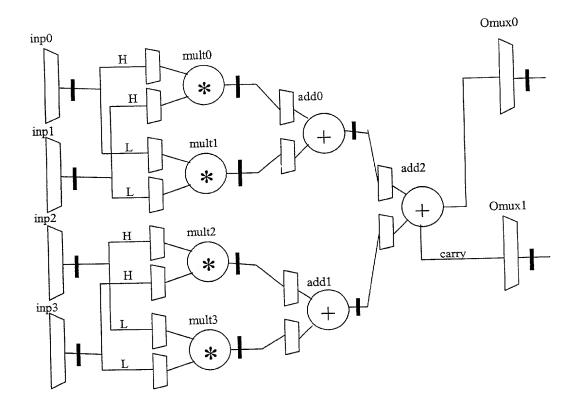
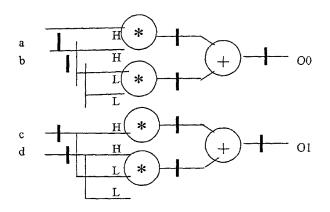


FIGURE 3E

4MULT2SUM – 2 Sums of 2 multipliers



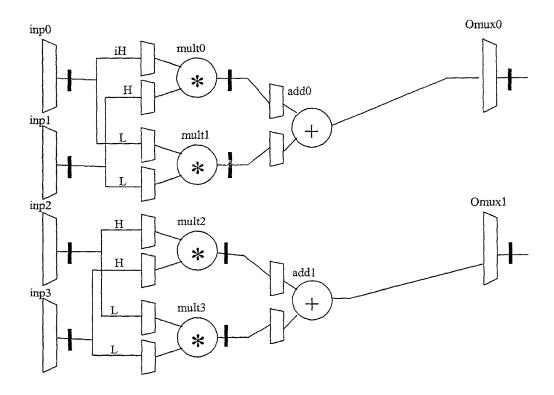
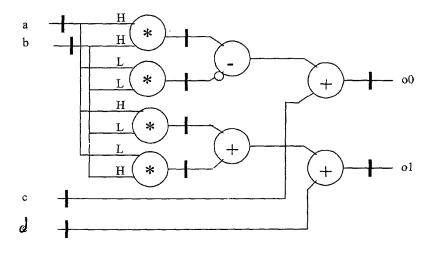


FIGURE 3F

CMULT-32-bit output complex multiply with 32-Bit accumulation input, Assumes real part in High 16-bits, imaginary in Low 16-bits



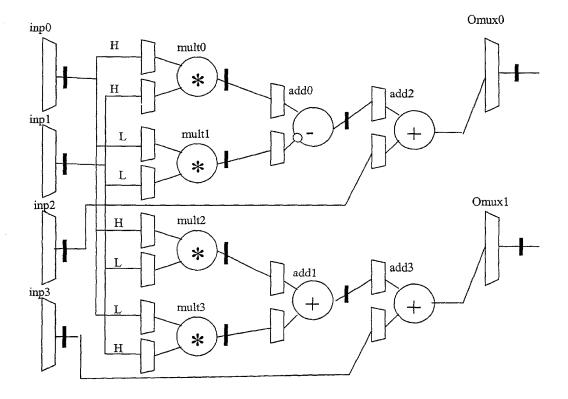
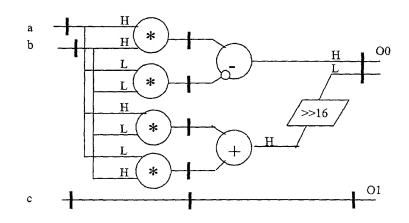


FIGURE 36

CMULT16 - Complex Multiplier with 16-Bit Packed data, and indepent delay path. Assumes real part in High 16-bits, imaginary in Low 16-bits



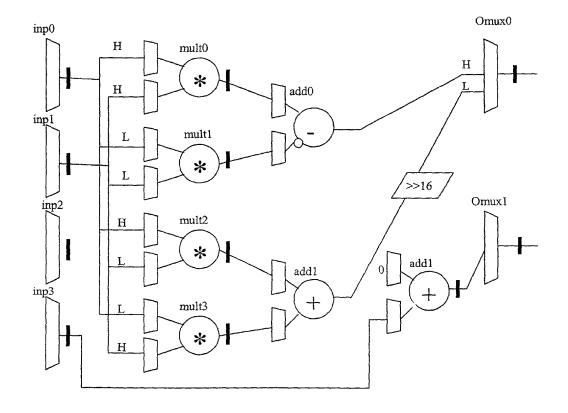


FIGURE 3H

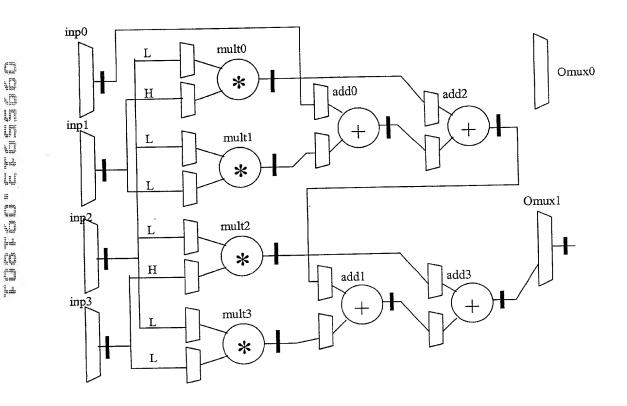


FIGURE 3I

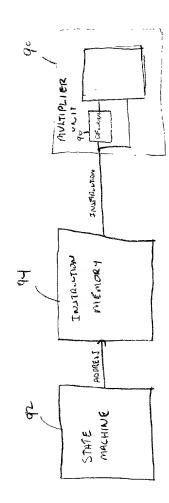




FIGURE 5

FIEURE 4

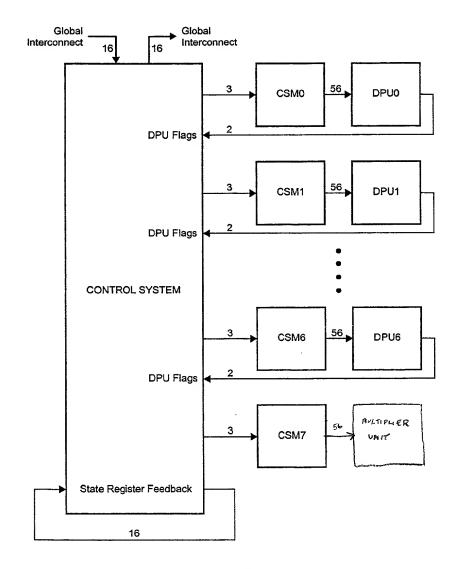


FIGURE 6

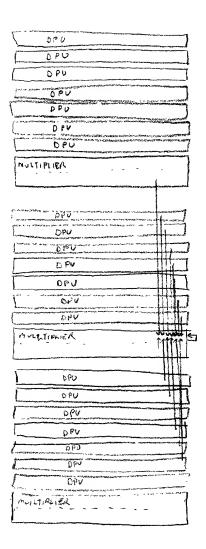


FIGURE 7

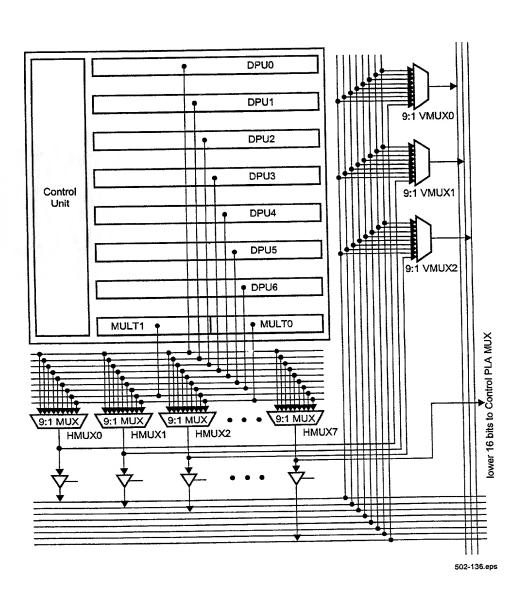


FIGURE 8

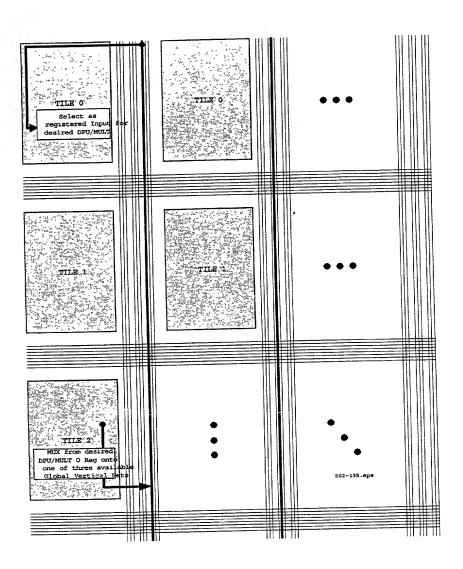


FIGURE 9

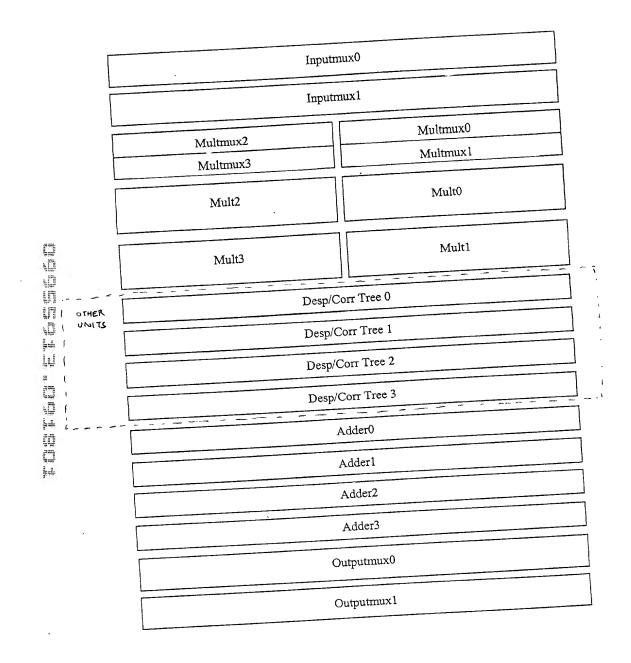


FIGURE 10

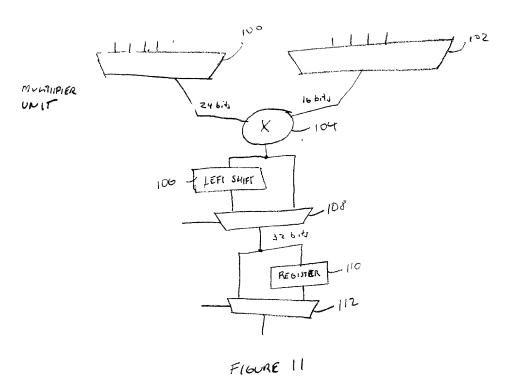


FIGURE 12

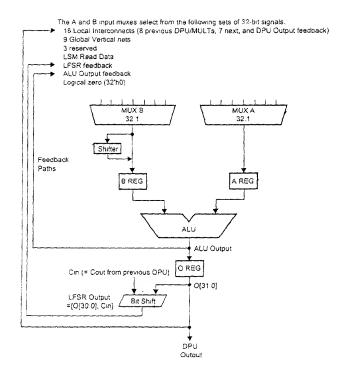


FIGURE 13